Amendments to the Abstract:

Please replace the previous Abstract with the following redlined Abstract:

~~The invention provides~~ A method and apparatus to reduce access time in synchronous FIFOs with zero latency overheads,~~.~~ ~~The~~ the apparatus including ~~FIFO buffer includes~~ a FIFO circuit capable of storing ~~'n'~~ data words, ~~each 'm' bits wide, having an 'm' bit wide data input terminal. Furthermore, the FIFO buffer includes~~ a read data set selection circuit connected to the data output terminals of the FIFO circuit and having two data output terminals providing simultaneous access to a selected storage location at an odd address and an even address. ~~An~~, an odd and even read ~~pointer generating~~ pointer-generating circuits ~~provides~~ provide ~~the~~ selection inputs to the data selection circuit ~~for selecting data at an odd read address of the read data selection circuit, while an even read pointer generating circuit provides the input for selecting data at an even read address. A multiplexer coupled to each of the two data output terminals of the read data set selection circuit selects one of its outputs as the final output of the FIFO. A~~, and a state controlling circuit coupled to ~~the~~ a multiplexer controls ~~the~~ selection of the final output and ~~this circuit also controls~~ the selection input to the read data set selection circuit for selecting an odd read address and an even read address.